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2 1. A semiconductor memory having mutually crossing word and bit lines at
3 which magnetoresistive memory cells are arranged, comprising:

4 a first magnetic layer having a first magnetization axis;

5 an insulating layer arranged in between; and

6 a second magnetic layer having a second magnetization axis, wherein the first
7 magnetic layer is formed from hard ferromagnetic material, the second magnetic layer is
8 formed from soft ferromagnetic material, and the first and the second magnetization axes
9 intersect if projected into a plane spanned by the word (8) and the bit line (9).

1 2. The semiconductor memory as claimed in claim 1, wherein the
2 magnetoresistive resistance is based on the tunnel magnetoresistive effect of the
3 combination of layer materials.

1 3. The semiconductor memory as claimed in claim 1, wherein the
2 magnetoresistive resistance is based on the giant magnetoresistive effect of the
3 combination of layer materials.

1 4. The semiconductor memory as claimed in claim 1, wherein the second
2 magnetization axis of the second magnetic layer is arranged parallel to a first of the word
3 or bit lines.

1 5. The semiconductor memory as claimed in claim 4, wherein the first
2 magnetization axis of the first magnetic layer is arranged perpendicular to the second
3 magnetization axis.

1 6. The semiconductor memory as claimed in claim 1, further comprising:
2 a circuit arrangement for evaluating the information content of at least one of the
3 magnetoresistive memory cells, the circuit arrangement having
4 - an AC current source, the AC current source being connected to the memory cell
5 via a word line;
6 a voltage measuring device, the voltage memory device being connected for
7 measuring the voltage to the word line and to the memory cell, via a bit line, the memory
8 cell being connected with a magnetoresistive resistance between the word and the bit line.

1 7. The semiconductor memory as claimed in claim 6, wherein the word line
2 connected to the AC current source is connected to a ground potential via an additional
3 resistance, and the resistance of the magnetoresistive memory cell has at least the
4 magnitude of the additional resistance.

1 8. The semiconductor memory as claimed in claim 7, wherein the word line
2 has an interconnect resistance, and the value of the additional resistance has at least the
3 value of the interconnect resistance.

1 9. The semiconductor memory as claimed in claim 6, wherein the voltage
2 measuring device has a unit for detecting a DC voltage component.

1 10. The semiconductor memory as claimed in claim 9, wherein the unit for
2 detecting a DC voltage component has at least one of a low-pass filter, an amplifier, a
3 comparator, and integration unit.

1 11. The semiconductor memory as claimed in claim 6, wherein the voltage
2 measuring device has a unit for the phase-selective measurement of voltage harmonics.

1 12. The semiconductor memory as claimed in claim 1, further comprising:
2 a circuit arrangement for evaluating the information content of at least one of the
3 magnetoresistive memory cells, the circuit arrangement having an AC voltage source, the
4 AC voltage source being connected to the memory cell via a word line, and a current
5 measuring device, the current measuring device being connected for a measurement of
6 the current flow between the bit line and a ground potential, one memory cell being
7 connected with a magnetoresistive resistance between the word and the bit line.

1 13. The semiconductor memory as claimed in claim 12, wherein the word line
2 connected to the AC voltage source is connected to a ground potential via an additional
3 resistance, and the magnetoresistive resistance of the memory cell has at least the
4 magnitude of the additional resistance.

1 14. The semiconductor memory as claimed in claim 13, wherein the word line
2 has an interconnect resistance, and the additional resistance has at least the value of the
3 interconnect resistance.

1 15. The semiconductor memory as claimed in claim 12, wherein the current
2 measuring device has a unit for detecting a DC current component.

1 16. The semiconductor memory as claimed in claim 15, wherein the unit for
2 detecting a DC current component has at least one of a low-pass filter, an amplifier, a
3 comparator, and an integration unit.

1 17. The semiconductor memory as claimed in claim 12, wherein the current
2 measuring device has a unit for the phase-selective measurement of current flow
3 harmonics.

1 18. A method for operating the semiconductor memory as claimed in claim 1,
2 for evaluating the information content of at least one of the magnetoresistive memory
3 cells, comprising:

4 feeding an AC current or an AC voltage having constant frequency and amplitude
5 into the word line connected to the memory cell to be evaluated;

6 measuring a signal during a measurement duration, the signal being derived from
7 the intensity of the current flow through the sequence of layers of the memory cell with a
8 magnetoresistive resistance by the current measuring device; and

9 evaluating the information content of the memory cell depending on the profile of
10 the signal during the measurement duration.

1 19. The method as claimed in claim 18, wherein the signal derived from the
2 measurement in the current or voltage measuring device includes the DC current or DC
3 voltage component of the measured AC current or AC voltage profile, and the evaluation
4 is carried out in a manner dependent on the sign of the DC current or DC voltage
5 component.

1 20. The method as claimed in claim 18 wherein, the signal derived from the
2 measurement in the current or voltage measuring device includes the first harmonic of the
3 AC current or AC voltage profile with double the AC current or AC voltage frequency
4 fed in, and the evaluation is carried out in a manner dependent on the sign of the
5 harmonic in the case of a predetermined phase.

1 21. The method as claimed in claim 20, wherein a phase-selective lock-in
2 technique is used.

1 22. The method as claimed in claim 18, wherein the measurement duration is
2 less than 20 nanoseconds.

1 23. The method as claimed in claim 18, wherein the AC current or AC voltage
2 frequency is more than 100 megahertz.

1 24. A method for operating the semiconductor memory as claimed in claim 1,
2 for evaluating the information content of at least one of the magnetoresistive memory
3 cells, comprising:

4 feeding an AC current or an AC voltage having constant frequency and amplitude
5 into the word line connected to the memory cell to be evaluated;

6 measuring a signal during a measurement duration, the signal being derived from
7 the voltage between the bit and the word line by the voltage measuring device; and

8 evaluating the information content of the memory cell depending on the profile of
9 the signal during the measurement duration.

1 25. The method as claimed in claim 24, wherein the signal derived from the
2 measurement in the current or voltage measuring device includes the DC current or DC
3 voltage component of the measured AC current or AC voltage profile, and the evaluation
4 is carried out in a manner dependent on the sign of the DC current or DC voltage
5 component.

1 26. The method as claimed in claim 24 wherein, the signal derived from the
2 measurement in the current or voltage measuring device includes the first harmonic of the
3 AC current or AC voltage profile with double the AC current or AC voltage frequency
4 fed in, and the evaluation is carried out in a manner dependent on the sign of the
5 harmonic in the case of a predetermined phase.

1 27. The method as claimed in claim 26, wherein a phase-selective lock-in
2 technique is used.

1 28. The method as claimed in claim 24, wherein the measurement duration is
2 less than 20 nanoseconds.

- 1 29. The method as claimed in claim 24, wherein the AC current or AC voltage
2 frequency is more than 100 megahertz.